a memory circuit which performs refresh operations of memory cells during an active state of a self refresh mode for refreshing said memory cells;

means for providing a chip active enable signal and a self refresh mode enable signal, said active state and a standby state of said self refresh mode being defined by said chip active enable signal and said self refresh mode enable signal; and

a substrate bias generator having a voltage pump circuit to boost a substrate voltage in response to an input of an oscillating signal generated in an oscillator, said substrate bias generator further comprising:

a substrate voltage level detector having said substrate voltage input thereto and outputting a signal which drives said oscillator in response to a substrate voltage level detected by said substrate voltage level detector[;], and

a controller having input thereto [a] said chip active enable signal, [a] said self refresh mode enable signal, and an output signal of said substrate voltage level detector, said controller controlling a switching operation of said substrate voltage level detector in

response to said substrate voltage level detected by said substrate voltage level detector, said controller also controlling said switching operation of said substrate voltage level detector in response to said chip active enable signal and said self refresh mode enable signal such that said substrate voltage level detector is not operative to drive said oscillator in [the] said stand-by state of [the] said self-refresh mode only when the detected substrate voltage level is a desired level.

2. (Twice Amended) A substrate bias generator of a semiconductor memory device having a voltage pump circuit to boost a substrate voltage in response to an input of an oscillating signal generated in an oscillator, said substrate bias generator further comprising:

a substrate voltage level detector having said substrate voltage input thereto and outputting a signal which drives said oscillator in response to a substrate voltage level detected by said substrate voltage level detector, said substrate voltage level detector comprising:

a first PMOS transistor whose source terminal is coupled to a power supply terminal and whose gate terminal is coupled to an output signal of [said] a controller,

first resistance means formed between said first PMOS transistor and a predetermined connecting node,

a second PMOS transistor whose source terminal is coupled to said connecting node and whose gate terminal is coupled to said substrate voltage,

second resistance means formed between said second PMOS transistor and a ground voltage terminal, and

an inverter having an input terminal coupled to said connecting node and outputting an output signal of said substrate voltage level detector; and

[a] said controller having input thereto a chip active enable signal, a self refresh mode enable signal, and said output signal of said substrate voltage level detector, said controller controlling a switching operation of said substrate voltage level detector in response to said substrate voltage level detected by said substrate voltage level detector.

4. (Twice Amended) A [substrate bias generator of a] semiconductor memory device comprising:

a memory circuit which performs refresh operations of memory cells [according to] during an active state of a self refresh mode for refreshing said memory cells[,];

means for providing a chip active enable signal and a self refresh mode enable signal, said active state and a standby state of said self refresh mode being defined by said chip active enable signal and said self refresh mode enable signal; and

[said] a substrate bias generator comprising:

a voltage pump circuit to supply a negative voltage to a substrate[;],

an oscillator to drive said voltage pump circuit[;],

a substrate voltage level detector to detect a level of said negative voltage and to drive said oscillator in response to said detected level[;], and

a controller circuit having input thereto [a] said chip active enable signal, [a] said self refresh mode enable signal, and an output of said substrate voltage level detector, an output of said controller circuit being input to said substrate voltage level detector, said output of said controller circuit being responsive to said chip active and said self refresh mode enable signals and said substrate voltage level detector output such that said substrate voltage level detector is not operative to drive said oscillator in [the] said standby state of [the] said self refresh mode only when the detected substrate voltage level is a desired level[;],

said substrate voltage level detector comprising:

a PMOS transistor having a gate coupled to said output of said controller circuit and having a source coupled to a power supply terminal, and